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Extremely Low-Cost Diagnostic Bio-Sensor using CMOS Technology for Medical Applications

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Abstract: *The advantages of CMOS sensors over conventional CCD sensors are the possibility in integration of all functions required for timing, exposure control, color processing, image enhancement, image compression, analog-to-digital (ADC) conversion on the same chip and low-power operation. However, although CMOS sensors naturally provide low-power dissipation, their wide utilization in various portable battery-operated devices generates an increased demand for more aggressive power reduction. This paper presents a CMOS image sensor architecture and reviews general considerations for power reduction in CMOS image sensors at all possible design levels - technology, device, circuit, logic, architecture, algorithm and system integration. The research and development of low-power miniature CMOS sensors triggers their penetration to various applications, such as bio-medical applications, digital still and video cameras, cellular phones, web and security cameras and many other applications.*

Keywords: *CMOS, CCD, micro-photodiodes, Photo-detectors, Light Emitting diodes.*

I. Introduction

During the last few years imaging systems for security applications have been significantly revolutionizing. Large, high cost and inefficient cameras mostly used for specific military and government applications have been replaced with compact, low-cost, low-power smart camera systems, becoming available not only for military and government, but for wide spreading in civilian applications. In this paper we will concentrate on major category: Biometrics systems – used for access control and person identification. Each of the presented categories requires sensors having different specifications: for example, while low-power and compactness are the most important features for some surveillance systems, robustness and high image quality are the most important requirement in biometric systems.

Medical applications also benefit from the fast image sensors technology development. Introduction of miniature, ultra-low power CMOS image sensors have opened new perspectives to minimally- invasive medical devices, like wireless capsules for gastrointestinal tract observation. Here we will review two very important medical applications:

(a) artificial retina – used as an artificial replacement or aid to the damaged human vision system,
(b) wireless capsule endoscopy – used in minimally invasive gastrointestinal tract diagnostics.

The remainder of the paper is organized as follows: Section II briefly presents CMOS image sensor technology with reference to CMOS image sensor architecture. The architecture of image sensors in security applications is described in Section II. Section IV reviews medical applications employing state-of-the-art CMOS imagers. Section V concludes the paper.

II. CMOS Image Sensor

ARCHITECTURE

Fig.1 shows the general architecture of a CMOS. A brief description of the main imager building blocks is presented herein.

A. Pixel Array – the imager pixel array consists of *N* by *M* pixels, while the most popular is the basic photodiode 3-T APS pixel, employing a photodiode and a readout circuit of three transistors: a photodiode reset transistor, a row select transistor and a source-follower transistor. Generally, many types of photo-detectors and pixels can be found in the literature. This includes a p-i-n photodiode, photo-gate and pinned photodiode based pixels, operating either in rolling shutter or in global shutter (snapshot) readout modes. The detailed description of these basic pixels can be found in. Pixel array power dissipation can vary from a hundreds of nWs for a small array employing 3 transistor APS architecture (making it almost negligible) to hundreds of mWs for large format "smart" imager employing in-pixel analog or digital processing.

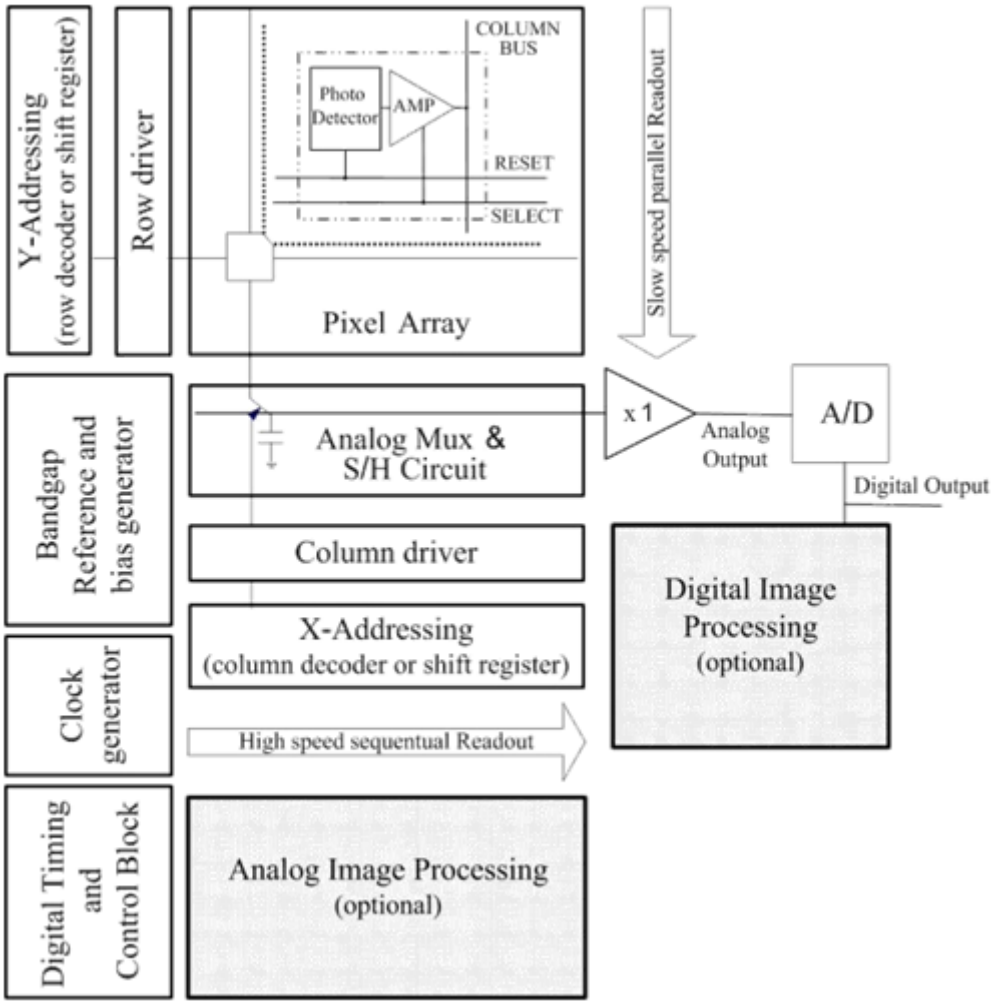


Fig.1. Architecture of CMOS SENSOR

B. Scanning Circuitry – Unlike CCD image sensors, CMOS imagers use digital memory style readout, usually employing Y-Addressing and X-Addressing to control the readout of output signals through the analog amplifiers and allow access to the required pixel. The array of pixels is accessed in the row-wise fashion using the Y-Addressing circuitry. All pixels in a row are read out into column analog readout circuits in parallel and then are sequentially read out using the X-Addressing circuitry. Generally, the Y-Addressing and X-Addressing circuitry can be implemented either using digital decoders or shift registers. The most acceptable solution is to use shift registers, because this solution reduces power dissipation and the number of global buses, compared to imagers, where decoders are used. An additional important role of shift registers in CMOS imagers is the regions (windows) of interest definition. A serial selection of regions of interest and their subsequent processing can greatly facilitate the computation complexity and significantly reduce power dissipation.

D. ***Analog Front End (AFE) –*** all pixels in a selected row are processed simultaneously and sampled onto S/H circuits at the bottom of their respective columns. Due to this column parallel process, for the array, having *M* columns, AFE circuitry usually consists of the *2*M* Sample and Hold (S/H) circuits, *M* size analog multiplexer, controlled by the X-Addressing circuitry, one or M amplifiers to perform correlated double sampling CDS (eliminates fixed pattern noise caused by random variations in the threshold voltage of the reset and pixel amplifier transistors, variations in the photo-detector geometry and variations in the dark current) and one or more analog variable gain amplifiers (VGA). These VGAs are usually used for color processing and for signal amplification for further analog processing or analog-to-digital conversion.

E. ***Analog-to-digital conversion (ADC)*** ADC is an inherent part of state-of-the-art "smart" image sensors. There are three general approaches to implementing sensor array ADC: (a) Pixel-level ADC, where every pixel has its own converter, (b) *Column-level ADC*, where an array of ADCs is placed at the bottom of the APS array and each ADC is dedicated to one or more columns of the APS array and (c) Chip-level ADC, where a single ADC circuit serves the whole APS array. The architecture, shown in Fig.1, utilizes this

approach for ADC implementation. Although many novel techniques for ADC were presented during the past few years, only a few of them were implemented in conjunction with CMOS image sensors. The most popular ADCs for imager applications are based on four fundamental architectures: successive approximation, sigma-delta, single-slope and pipelined architecture. The pixel-level approach is suitable for simple sigma-delta, single slope and modifications of successive approximation ADCs. Single-slope, sigma-delta and successive approximation ADCs can be implemented as column-level ADCs. Finally, successive approximation and pipelined ADCs are suitable for the chip-level approach. Usually, the sigma-delta and successive approximation ADCs are considered to be power efficient architectures.

E. ***Bandgap reference and current generators*** **–** these building blocks are used to produce on-chip analog voltage and current references for other building blocks like amplifiers, ADCs, digital clock generators and others. The power, dissipated in bias circuitry is wasted and should be in principle minimized. However, inadequate bias schemes may increase the noise and therefore require proportional increase in power. For example, a bias current would be noisier if it is obtained by multiplying a smaller current. In many large format imagers, power dissipation of the bandgap and current generators can be neglected. Usually, the maximum power dissipation of a few tens of μWs is achieved.

F. ***Digital timing and control block, clock generator*** **-** aim to control the whole system operation. Their implementation on the chip level decreases the number of required I/O pads and thus reduces system power dissipation. Synchronized by the generated clock, the digital timing and control block produces the proper sequencing of the row address, column address, ADC timing and the synchronization pulses creation for the pixel data going off chip. In addition, it controls the synchronization between the imager and the analog and digital processing. Digital timing and control block are digital circuits, and therefore their power dissipation can be analyzed in a similar way as it is done in standard digital circuits.

G. ***Analog and Digital Image Processing*** **–** Both analog and digital processing can be performed either in the pixel or in the array periphery. There are advantages and disadvantages for both methods. *In-pixel digital image processing* is very rare because it requires pixel-level ADC implementation and results in very poor fill factor and large pixel size. *In-pixel analog image processing* is very popular, especially in the field of neuromorphic vision chips. In these chips in-pixel computations are fully parallel and distributed, since the information is processed according to the locally sensed signals and data from the pixel neighbors. Some neuromorphic visual sensors operate in the sub-threshold region and therefore have very low- power dissipation. The in-pixel analog image processing implementation usually results in increased pixel size, but allows more efficient computation. Other applications employing in-pixel analog processing are tracking chips, wide dynamic range sensors, motion and edge detection chips, compression chips and others.

H. ***The periphery analog processing*** approach assumes that analog processing is performed in the array periphery without penalty on the imager spatial resolution and it is usually done in a column parallel manner. While this approach has computational limitations compared to in-pixel analog processing, it provides several significant benefits, like area saving, reuse of the processing circuits for better matching and potentially has more pixels. Periphery digital processing is the most standard and usually simpler. It is performed following the A/D conversion, utilizes standard existing techniques for digital processing and is usually done on the chip level. The main disadvantage of this approach is its inefficiency by means of area occupied and power dissipation.

III. CMOS Image Sensor Technology In A Glance

The continuous advances in CMOS technology for processors and DRAMs have made CMOS sensor arrays a viable alternative to the popular charge-coupled devices (CCD) sensor technology. Standard CMOS mixed-signal technology allows the manufacture of monolithically integrated imaging devices: all the functions for timing, exposure control and ADC can be implemented on one piece of silicon, enabling the production of the so-called "camera-on-a-chip". The traditional imaging pipeline functions such as color processing, image enhancement and image compression can also be integrated into the camera. This enables quick processing and exchanging of images. The unique features of CMOS digital cameras allow many new applications, including network teleconferencing, videophones, guidance and navigation, automotive imaging systems, robotic and machine vision and of course, security and bio-medical image systems.

Most digital cameras still use CCDs to implement the image sensor. State-of-the-art CCD imagers are based on a mature technology and present excellent performance and image quality. They are still unsurpassed for high sensitivity and long exposure time, thanks to extremely low noise, high quantum efficiency and very high fill factors. Unfortunately, CCDs need specialized clock drivers that must provide clocking signals with relatively large amplitudes (up to 10 V) and well-defined shapes. Multiple supply and bias voltages at non-standard values (up to 15 V) are often necessary, resulting in very complex systems.

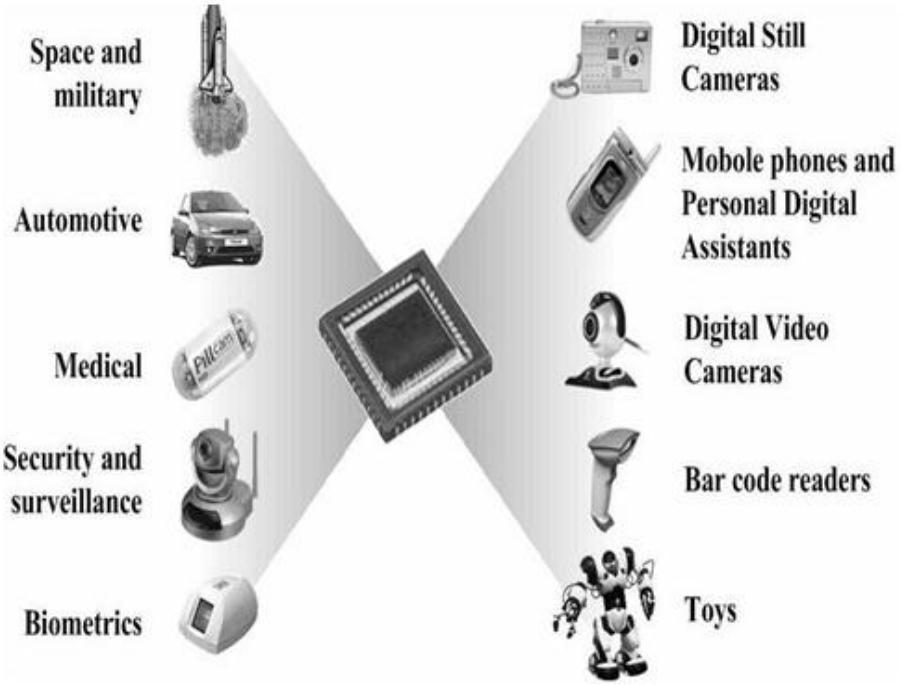


Fig.2. CMOS sensors applications

IV. CMOS Sensor In Medical Applications

A. Biometric personal identification

Biometric personal identification is strongly related to security and it refers to "identifying an individual based on his or her distinguishing physiological and/or behavioral characteristics (biometric identifiers)".

Usually, conventional image sensors with external hardware or software image processing are used. The difficulty for on-chip integration is caused by the complexity of the required image processing algorithms. However, there are some developments that successfully achieve the required goals by parallel processing utilization. To give some more detailed examples in the field, we concentrate on fingerprint sensors. Generally these sensors can be classified by the physical phenomena used for sensing: optical, capacitance, pressure and temperature. The first two classes are the most popular and both mainly employ CMOS technology.

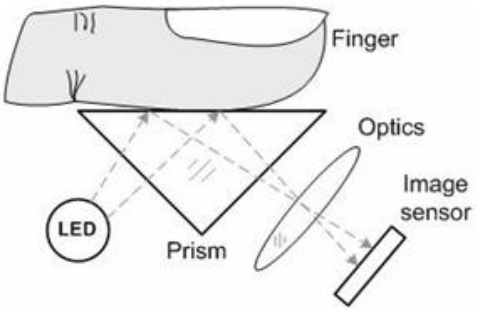
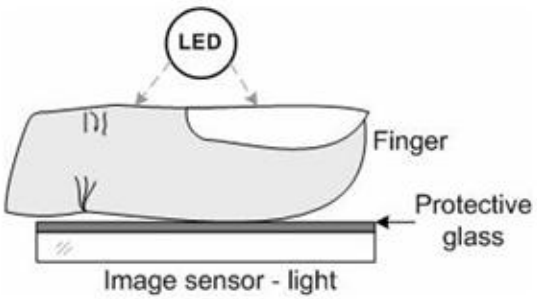
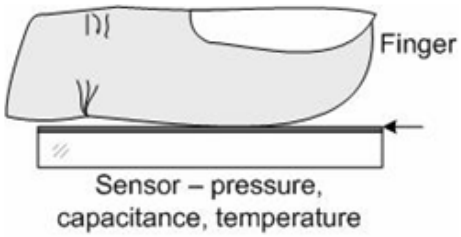


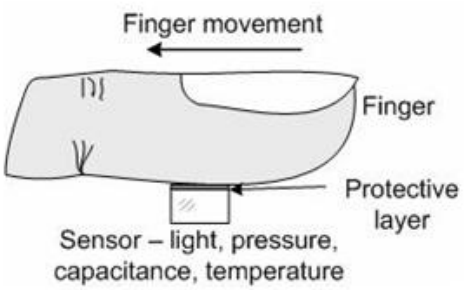
Fig.3(a) optical - reflection based sensor



(b) optical – transmission based sensor



(c) non-optical – based on pressure capacitance or temperature sensor



(d) sweep sensor

The most popular approach (see Fig.3 (a)) is based on optical sensing and light reflection from the finger surface. Also, this type provides high robustness to finger condition (dry or wet), but the system itself is tend to be bulky and costly. Alternative solutions that can provide compact and lower cost solutions, are based mostly on solid state sensors where the finger is directly placed on the sensor. However, in these solutions the sensor size needs to be at least equal to the size of the finger part used for sensing. Two sensors of this type are shown in Fig. 3 (b) and (c). The first one is based on light transmitted through the finger and then sensed by the image sensor, while the second one is the non-optical sensor that can be implemented either as pressure, capacitance or temperature sensor. The fingerprint sensor, known as a "sweep" sensor and shown in Fig.3(d), can be implemented using either the optical or other previously mentioned techniques. A "sweep" sensor employs only a few rows of pixels, thus in order to get a complete fingerprint stamp the finger needs to be moved over the sensing part. Such technology greatly reduces the cost of the sensor due to reduced sensor area and solves the problem of fingerprint stamp that needs to be left on the surface in the first two methods.

In all presented methods, the output signal is usually an image and the sensors are composed of pixels that sense either temperature, pressure, photons or change in capacitance. The overall architectures of these sensors are similar to the architecture described in section II and they integrate various image and signal processing algorithms, implemented the same die. Various research papers have been published in this area and numerous companies are working on such integration. For example, in the authors implement image enhancement and robust sensing for various finger conditions. Capacitive sensing CMOS technology is used and data is processed in a column parallel way. The same technology is used also in, but the fingerprint identifier is also integrated and the data is processed massively in parallel for all pixels.

Despite the fact that fingerprint technology is quite mature, there is much work to be done to reduce power consumption, to improve technology and image processing algorithms and to achieve better system miniaturization.

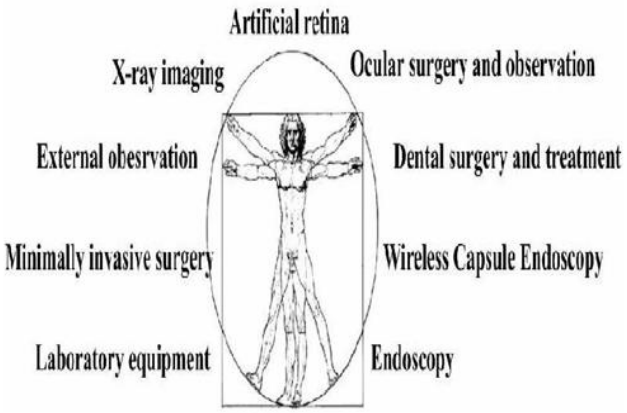


Fig.4 Image sensors applications in medicine

B. Wireless Capsule Endoscopy

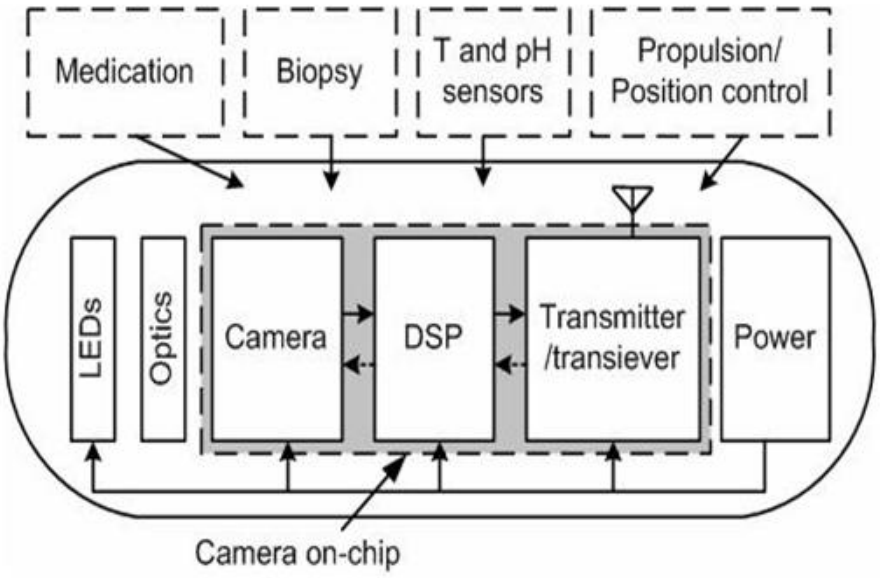


Fig.5 The swallow capsule architecture

Conventional medical instrumentation for gastrointestinal tract observation and surgery uses an endoscope that is externally penetrated. These systems are well developed and provide a good solution for inter-body observation and surgery. However, the small intestine (bowel) was almost not reachable using this conventional equipment, leaving it for observation only through surgery through inconvenient and sometimes painful push endoscopy procedures. Few years ago the sphere was revolutionized by the invention of the wireless image sensor capsule, which after swallowing, constantly transmits a video signal during its travel inside the body. The capsule movement is insured by the natural peristalsis. According to Gavriel Iddan , the founder of Given Imaging that commercializes this technology, "The design of the video capsule was made possible by progress in the performance of three technologies: complementary metal oxide silicon (CMOS) image sensors, application-specific integrated circuit (ASIC) devices, and white-light emitting diode (LED) illumination".

The general architecture of the capsule is shown in the Fig.5. It consists of LEDs, optics, camera, digital system processing, transmitter or transceiver and a power source. The dashed blocks represent additional future requirements for such capsules.

All capsule electronic components are required to be low power consumers to enable constant video transmission for a prolonged time (for about 6-8 hours) and/or high capacity batteries. An alternative solution to in-capsule batteries is to use an external wireless power source that supplies energy to the capsule through electromagnetic coils. Such a solution enables to relax power requirements for the capsule electronics. This solution also provides an advantage in freeing space inside the capsule for other useful functions such as biopsy or medication. Also, the capsule position can be controlled externally through a strong magnetic field. But the required strong magnetic field can limit the capsule usage in spite of position control advantages.

Currently the Given Imaging capsule developers have reached very encouraging results enabling two capsules: one intended for the Esophagus part (the upper part) of the gastrointestinal tract and the second for small intestine observation. The first kind of the capsule is equipped with two CMOS image sensors and can transmit the video signal for about 20 minutes with 14 frames per second for each camera. The second one consists of only one CMOS image sensor and can transmit two frames per second for about eight hours. The company is developing now a new capsule generation that can transmit four frames per second.

Despite these encouraging results, a lot of work should be done to allow further miniaturization, image processing and compression algorithms integration, power reduction by various means (system integration, technology scaling etc.), frame-rate increase, quality improvement and usage of alternative power sources with larger capacity. The ultimate goal that needs to be achieved is full video frame-rate transmission for about 7-8 hours. To achieve these goals, a number of additional research groups work worldwide on wireless capsules development: eStool by Calgary university in Canada, MiRO by Intelligent Microsystems Center in Korea , EndoPill by Olympus.

C. Artificial Retina

Artificial vision is another example of CMOS image sensors implementation in medical applications. Today millions of people are suffering from full or partial blindness that was caused by various retinal deceases. In the early eighties it was shown that electrical stimulation of the retinal nerves can simulate visual sensation even in the patients with fully degraded receptors. Recently, researchers in a number of research institutes have developed miniature devices that can be implanted into the eye and stimulate the remaining retinal neural cells, returning partial vision ability for the blind patients. Such implants are called artificial retinas. Usually they are implanted in the macula area that normally is densely populated by the receptors and enables high-resolution vision. This break-through was enabled by the progress in electronics, surgical instrumentation, and biocompatible materials. Currently there are two major approaches for artificial retina development. The first and the most promising one is the integration of sensing and stimulation elements in the same device and the second is separation of sensing and stimulation.

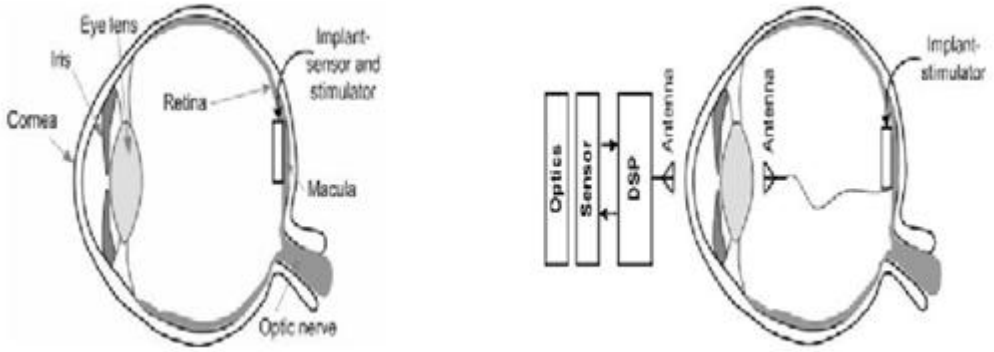


Fig.6 Artificial retinas

In the first approach, an artificial retina device is an autonomous circuitry that does not require external control and the optics that is used for sensing is the natural optics of the eye composed of the cornea and lens. In the second, all the sensing and processing is performed outside of the eye and only stimulating elements are implanted during surgery. The data transfer from the sensing part to the stimulation part is performed through an RF link or through a tiny cable. In both approaches the implant can be subretinal or epiretinal.

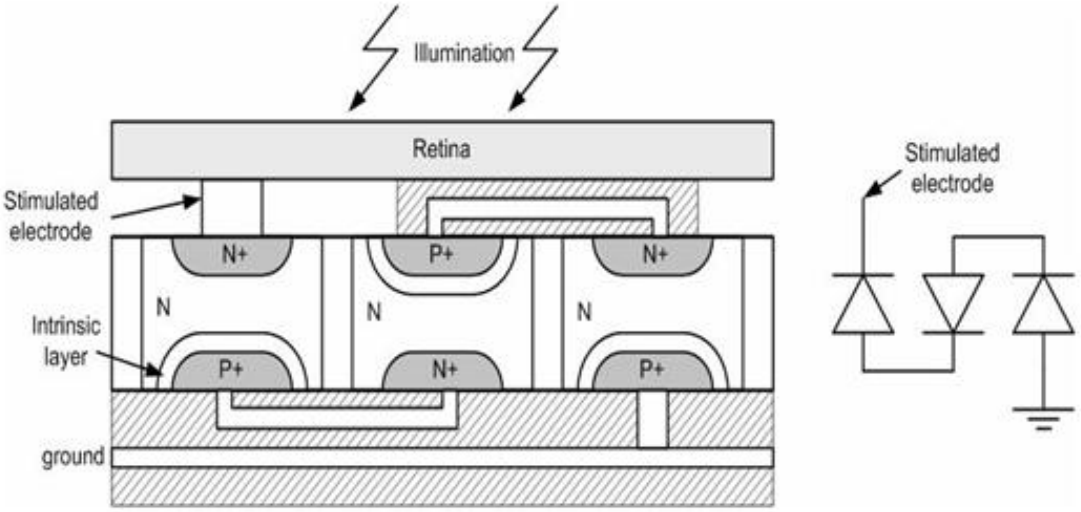


Fig.7 Artificial silicon retina – basic unit

Actually there is a number of groups working in the field but we will concentrate on two that have shown very promising results and are now performing clinical trials and commercialization through companies named Optobionics and Second Sight. Both groups already have a number of patients with such implants.

The device developed by Optobionics group does not require any power source, integrates about 5000 sensing (micro-photodiodes) and stimulation (electrodes) elements, features two millimeters in diameter and is implanted under retina. The basic artificial silicon retina unit is shown in Fig.6. It is composed of a stimulating electrode and three PIN photodiodes connected in series to increase the output voltage.

V. Conclusion

In this paper the motivation for research and development in CMOS was presented. A general architecture of a CMOS imager was shown. An approach for CMOS sensors in various applications at different design levels was presented. Although we couldn't provide more detailed explanations on existing low-power design techniques due to the limited space available, we hope we have succeeded in presenting general concepts that can be useful to beginners in the area of image sensors design.

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